REMARKS

Summary Of Office Action

Claims 1-53 are pending in this application.

Claims 1, 2, 6, 13-15, 18, 25, 31, 35, 43, 44, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") in view of Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

Claims 3-5, 7-12, 16, 17, 19, 20, 26-30, 32-34, 36-39, 41, 45-47, 49, 50, and 51-53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig in further view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson").

Claims 21 and 40 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig in further view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 22-24 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig in further view of Hartwell in further view of Johnson.

Reconsideration of this application in view of the following remarks is respectfully requested.

Rejections of Claims Under 35 U.S.C. § 103(a)

Claims 1-2, 6, 13-15, 18-25, 31, 35, 43, 44, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig. Claims 3-5, 7-12, 16, 17, 19, 20, 26-30, 32-34, 36-39, 41, 45-47, 49, 50, and 51-53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig in further view of Johnson. Claims 21 and 40 were rejected under 35 U.S.C. § 103(a) as being

obvious from Stevens in view of Olarig in further view of Hartwell. Claims 22-24 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig in further view of Hartwell in further view of Johnson. These rejections are respectfully traversed.

I. Rejections of Independent Claims 1, 13, 25, 31, and 43

Applicant's invention, as defined by independent claims 1, 13, 25, 31, and 43 is directed toward a method, computer systems, a memory controller, and an apparatus, respectively, for selecting an operating speed of a memory module interface. Applicant's invention counts the number of memory modules, generates multiple clock frequencies to provide selectable operating speeds for the memory module interface, and selects one of the operating speeds for the memory module interface in accordance with the counting.

Stevens is directed to a method for configuring or initializing a memory device. During configuration or initialization, a clock generator is started in the memory controller. The frequency of the clock is generated by "determining a channel frequency at which all [memory modules] may operate" (Stevens, column 13, lines 43-45; emphasis added).

Olarig is directed to a memory controller supporting DRAM circuits that can each operate at a different frequency. Upon initialization, the computer system determines the type of DRAM circuits present and provides status information to the memory controller which, in response, generates multiple clock signals with appropriate frequencies that are respectively applied to the DRAM circuits.

The Examiner asserts that the combination of Stevens and Olarig shows all of the elements of applicant's independent claims 1, 13, 25, 31, and 43. Applicant respectfully disagrees.

In particular, neither Stevens nor Olarig discloses or suggests "selecting one of the operating speeds of said memory module interface" (emphasis added) as required by applicant's independent claims.

Stevens, as the Examiner correctly acknowledges, does not disclose or suggest generating multiple clocks at different frequencies to provide the selectable operating speeds.

Olarig does not disclose or suggest selecting one of the multiple generated clock signals for the memory module interface. Instead, Olarig discloses "a memory controller [that] generates multiple clock signals for use by the different SDRAM memory devices" (Olarig, column 3, lines 15-18).

Olarig uses multiple clock signals for its SDRAM memory devices.

In contrast, applicant's invention requires selection of one of the generated clock frequencies for use by the memory module interface.

Furthermore, neither Stevens nor Olarig discloses or suggests selecting the operating speed in accordance with the counting of the number of memory modules.

Both Stevens and Olarig disclose the generation of one or more clock speeds based on the speed of the memory modules, but not on the number of memory modules as required by applicant's independent claims.

Thus, neither Stevens nor Olarig discloses or suggests these limitations of applicant's claims.

Moreover, neither Stevens nor Olarig provides a motivation for being combined with the other. Although both Stevens and Olarig relate to memory controller systems which may contain memory devices that operate at different speeds, Stevens and Olarig disclose contrary techniques for addressing this problem.

Stevens' system "determin[es] a [i.e., one] channel frequency at which all [memory devices] may operate" (Stevens, column 13, lines 43-45).

In contrast, Olarig's system "generates multiple clock signals with appropriate frequencies for use by the SDRAM memory devices" (Olarig, abstract, lines 3-5).

Thus, Stevens generates a single clock signal of appropriate frequency for the memory controller while Olarig generates a different clock signal for each memory device.

Thus, there is no motivation to combine Stevens and Olarig -- and even if there were -- the combination of Stevens and Olarig still does not result in applicant's invention as defined in independent claims 1, 13, 25, 31, and 43.

II. Rejections of Independent Claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13, 25, 31, and 43 in further view of Johnson shows all of the elements of applicant's independent claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53. Applicant respectfully disagrees with the Examiner's assertion.

The application of Johnson for the alleged teaching of the additional elements of claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53 does not make up for the deficiencies of Stevens and Olarig. In particular, Johnson does not teach or

suggest the generation of multiple clock frequencies and the selection of one of them for the memory module interface. Thus, for at least the reasons discussed above with respect to the patentability of claims 1, 13, 25, 31, and 43, applicant respectfully submits that independent claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53 are also not rendered obvious by the combination of Stevens and Olarig in further view of Johnson.

III. Rejections of Independent Claims 21 and 40

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13, 25, 31, and 43 in further view of Hartwell shows all of the elements of applicant's independent claims 21 and 40. Applicant respectfully disagrees with the Examiner's assertion.

The application of Hartwell for the alleged teaching of the additional elements of claims 21 and 40 does not make up for the deficiencies of Stevens and Olarig. In particular, Hartwell does not teach or suggest having at least two PLLs to generate respective clock signals of different frequencies and providing one of the clock signals to the memory module interface. Thus, for at least the reasons discussed above with respect to the patentability of claims 1, 13, 25, 31, and 43, applicant respectfully submits that independent claims 21 and 40 are also not rendered obvious by the combination of Stevens and Olarig in further view of Johnson.

IV. Rejections of Independent Claims 23, 24, and 42

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13,

25, 31, and 43 in further view of Hartwell and in further view of Johnson shows all of the elements of applicant's independent claims 23, 24, and 42. Applicant respectfully disagrees with the Examiner's assertion.

The application of Hartwell and Johnson for the alleged teaching of the additional elements of claims 23, 24, and 42 does not make up for the deficiencies of Stevens and Olarig. In particular, Hartwell and Johnson do not teach or suggest suggest having at least two PLLs to generate respective clock signals of different frequencies and providing one of the clock signals to the memory module interface. Thus, for at least the reasons discussed above with respect to the patentability of claims 1, 13, 25, 31, and 43, applicant respectfully submits that independent claims 23, 24, and 40 are also not rendered obvious by the combination of Stevens and Olarig in further view of Hartwell in further view of Johnson.

V. Rejections of Dependent Claims

For at least the reasons discussed above with respect to independent claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40-43, and 51-53, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40-43, and 51-53 are also not rendered obvious from the combination of Stevens, Olarig, Johnson, and Hartwell (i.e., dependent claims are patentable if their independent claim is patentable).

* * *

Accordingly, applicant respectfully requests that the rejections of claims 1-53 under 35 U.S.C. § 103(a) be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-53 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,

Michael J. Chasan
Registration No. 54,026
Agent for Applicant

FISH & NEAVE LLP
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020-1105
(212) 596-9000